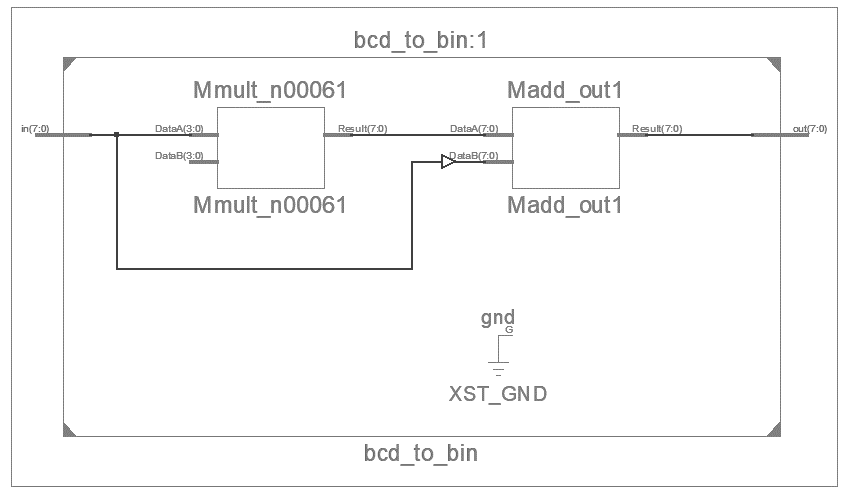
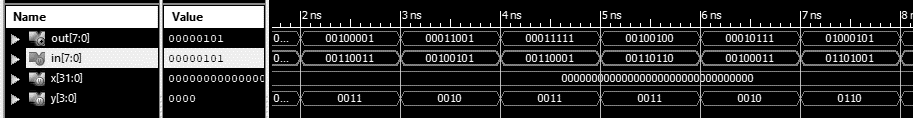
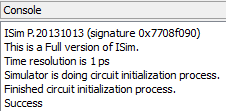
**RTL Diagram:**

****

**Output Waveform:**

****

**Simulation Output:**

****

**Experiment-3**

**Objective:**

To design a BCD to binary converter and write a simple test bench for it. The test bench should generate stimulus to completely verify the functionality of the design.

**Tool Used:**

Xilinx ISE.

**Theory:**

The value of 2nd digit is multiplied with 10 and added to the lower bit.

**Design Code:**

module bcd\_to\_bin(input [7:0]in, output [7:0]out);

    assign out = in[7:4]\*10 + in[3:0];

endmodule

**TB Code:**

module tb();

reg [7:0]in;

    wire [7:0] out;

    integer x=0;

      reg [3:0] y;

    bcd\_to\_bin dut(in,out);

    initial begin

        repeat(10)begin

                y = $random;

                if (y > 9) y = y+6;

                in[3:0] = y;

                y = $random;

                if (y > 9) y = y+6;

                in[7:4] = y;

                #1;

            if(out != in[7:4]\*10 + in[3:0]) x = x+1;

        end

        if(!x) $display("Success");

        else $display("Failure");

    end

endmodule

**Result:**

The simulation output and the RTL diagram is observed and found to be valid.